Remarks

Claims 1, 6, 9, 13, 14, 17, 21 and 24 are amended. Claims 26 - 29 are added. No claims are cancelled. Reexamination and reconsideration of this application, as amended, are respectfully requested.

The Examiner rejected claims 24 and 25 under 35 USC § 112 as not providing sufficient antecedent basis to independent base claim 17. The applicant has amended claim 24 to properly reference independent base claim 17 and respectfully submits that claims 24 and 25 now have sufficient antecedent basis.

The Examiner rejected claim 1 as being anticipated by U.S. Patent No. 5,734,847 to Garbus et al. (the "'847 patent") under 35 USC § 102(b). This rejection is respectfully traversed.

The specification of the present application relates to, among other things, a peripheral device coupled to a data bus which defines a plurality of "device functions." The device functions are accessible through a single interface coupling the peripheral device to the data bus. A first processing system coupled to the data bus may address bus transactions to a first of the device functions and a second processing system coupled to the data bus may address bus transactions to a second of the device functions. [Specification, para. 24] Accordingly, the first and second processing systems may each access different device functions defined by a single peripheral device.

The device shown in the '847 patent appears to show an I/O processor 5 coupled between a primary PCI bus 7 and a secondary PCI bus 15, and a host processor 3 coupled to the primary PCI bus 7. Separate PCI devices 11 and 13 are also coupled to the secondary PCI bus 15. The I/O processor 5 may cause either of these PCI devices to be undetectable by the host processor 3 to thereby establish "private" devices. Accordingly, the host processor 3 and I/O processor 5 may each be adapted to communicate with different, distinct PCI devices on the secondary bus. ['847 patent, Figure 1 and col. 8, ll. 20 – 32]

Claim 1 distinguishes over the device shown in the '847 patent by reciting, among other things:

> a first processing system adapted to communicate with a ***first device function*** defined by the peripheral device through the data interface; and
>
> a second processing system adapted to communicate with a ***second device function*** defined by the peripheral device through the data interface. [emphasis added]

Merely showing different PCI ***devices*** that may be configured to communicate with different, distinct processors on a PCI bus, the '847 patent does not disclose, suggest or make obvious a "first processing system adapted to communicate with a first ***device function***" and a "second processing system adapted to communicate with a ***second device function***" where the first and second device functions are ***defined by the same peripheral device***. Accordingly, the applicant respectfully submits that claim 1, and claims 2 – 8 depending therefrom, distinguish over the '847 patent. While differing in scope from claim 1, claim 9 recites limitations which are similar to those in claim 1 which are quoted above. Accordingly, the applicant respectfully submits that

claim 9, and claims 10 through 16 depending therefrom, similarly distinguish over the device shown in the '847 patent.

Claim 5 further distinguishes over the device shown in the '847 patent by reciting, among other things:

> logic to cause the peripheral device to conceal one or more ***device functions*** from the second processing system while enabling the second processing system to communicate with at least one unconcealed device function defined by the peripheral device.

Merely showing an I/O processor 5 capable of defining a PCI device that is undetectable by the host processor 3, the '847 patent does not disclose, suggest or make obvious concealing "one or more ***device functions*** . . . while enabling the second processing system to communicate with ***at least one unconcealed device function***" as set forth in claim 5. Accordingly, the applicant respectfully submits that claim 5, and claims 6 – 8 depending therefrom, further distinguish over the '847 patent. While differing in scope from claim 5, claims 13 through 16 recite limitations similar to those in claim 5 which are quoted above. Accordingly, the applicant respectfully submits that these claims similarly distinguish over the device shown in the '847 patent.

The Examiner also rejected claim 17 as being obvious in view of the '847 patent and U.S. Patent No. 5,737,344 to Belser (the "'344 patent") under 35 USC § 103(a). This rejection is respectfully traversed.

The specification of the present application also relates to an I/O processor 14 capable of communicating with a peripheral device 16 using bus transactions. The I/O processor 14 may initiate one or more bus transactions to configure one or more device functions defined by the peripheral device 16. The I/O processor 14 may then initiate

bus transactions to conceal at least some of the configured device functions from subsequent bus transactions initiated by a host processor 12. Accordingly, the host processor 12 may only configure resources to communicate with the unconcealed device functions. [Specification, para. 27]

Claim 17 distinguishes over the device shown in the '847 patent by reciting, among other things:

> initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures ***while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure***. [emphasis added]

The device shown in the '847 patent, merely showing an I/O processor 5 that is capable of concealing an entire PCI device from a host processor 3, does not disclose, suggest or make obvious causing "a first device function to be concealed from subsequent enumeration procedures ***while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure***." Accordingly, the applicant respectfully submits that claim 17 distinguishes over the device shown in the '847 patent. The '344 patent, apparently showing a processor that executes machine-readable instructions stored on a direct access storage device, does not make up for the deficiencies of the '847 patent in meeting the above quoted limitations. Accordingly, the applicant respectfully submits that claim 17, and claims 18, 19 and 20 depending therefrom, distinguish over the combination of the '847 and '344 patents.

While differing in scope from claim 17, claim 21 includes limitations similar to those in claim 17 which are quoted above. Accordingly, the applicant respectfully

submits that claim 21, and claim 22 through 25 depending therefrom, similarly distinguish over the combination of the '847 and '344 patents.

The applicants respectfully submit that the application is now in form for allowance. Reconsideration of this case is respectfully requested. Please charge Deposit Account #02-2666 for the addition of claims and any other fee payment deficiencies associated with this case. If the Examiner finds that this case is in any way not in proper form for allowance, the applicants request that the Examiner contact the applicants' representative at (310) 252-7621.

Respectfully submitted,

Schmisseur

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